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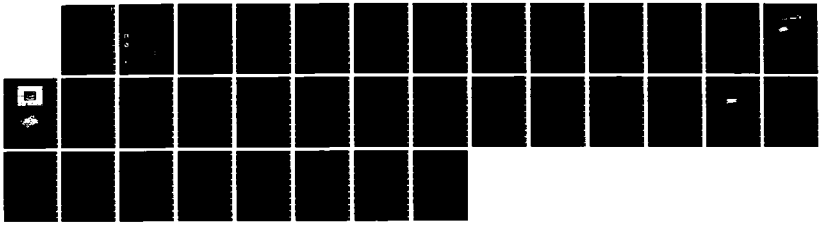

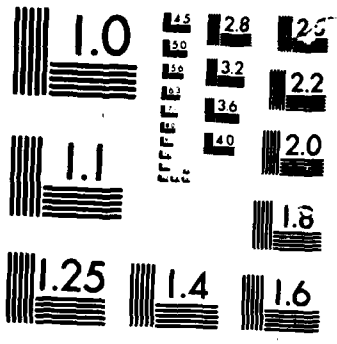

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Design of the AFGL Prototype Long Baseline Tiltmeter

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SCHARINE KIRCHOFF

29 August 1985

EARTH SCIENCES DIVISION PROJECT 2309
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HANSCOM AFB, MA 01731

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This report describes the design of a prototype long baseline tiltmeter that has been built and tested. A discussion of the mechanical tank and interferometer system, sensor electronics and interface, and the computer system is included. Results of a two-day test are described. The prototype tiltmeter shows a high dependence upon temperature variation. This must be eliminated if the tiltmeter is to be reliable over long periods of time.

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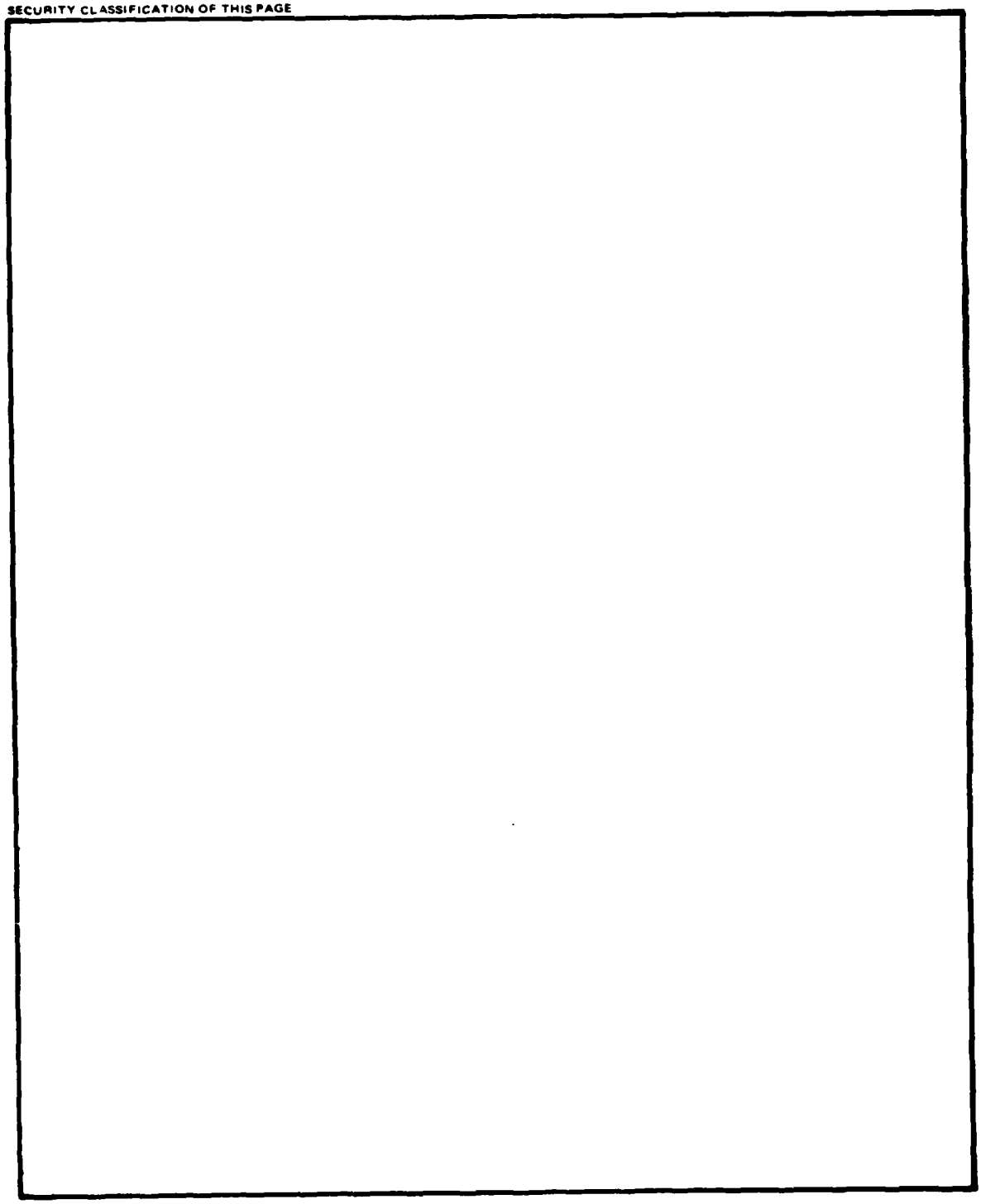

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1. INTRODUCTION

The spatial distribution and magnitude of crustal tilt remains largely unknown. Information on crustal tilt comes primarily from repeated historic geodetic measurements and tide gauge observations. While these measurements provide some constraints on the nature of regional crustal tilt, they do not have the spatial and temporal resolution required for many applications. For example, it is unlikely that such measurements can provide information on localized ground deformation in the vicinity of strategic Air Force facilities. It is important, however, to monitor such movements since they can impact navigation systems over relatively short time periods. Tilt measurements may prove useful for forecasting possible destructive earthquake activity in such areas.

A group at the Solid Earth Geophysics Branch of the Air Force Geophysics Laboratory has been actively involved in building and testing borehole tiltmeters in order to establish the long-term stability of individual tiltmeters and the coherence between closely spaced borehole tiltmeter arrays.[1-3] In addition, comparisons have been made between borehole tiltmeters at various depths and a 500-m long baseline tiltmeter.[4] The results of these studies have shown that

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(Received for Publication 26 August 1985)

References 1 to 4 will not be listed here. See References, page 27.

borehole tiltmeters at shallow depths (≤ 3 m) are plagued with short duration rainfall, temperature, and thermoelastic effects that can contribute to long-term mechanical drift.[2] Deep borehole tiltmeters (≥ 30 m) are more stable and are less affected by near-surface noise. An AFGL deep borehole tiltmeter was favorably compared to the 500-m long baseline tiltmeter that was optically anchored 30 ft below the surface to give an extremely low drift rate.[4] This demonstrated that deep borehole tiltmeters can give stable results; however, high costs for a tiltmeter and the drilling of a borehole are inevitable.

In an effort to meet the needs of the Air Force for a relatively inexpensive, stable, and transportable tiltmeter, the Solid Earth Geophysics Branch has designed and built a 1-m prototype long baseline tiltmeter, which is described in this report. A long baseline tiltmeter was chosen, rather than a borehole tiltmeter, because of its ability to spatially average near-surface noise and for the installation cost savings in not having to drill a borehole. The prototype baseline was kept relatively short (1 m) in order to keep the tiltmeter transportable (small size), keep its time constant low (on the order of several seconds), and for the purpose of testing the stability and sensitivity of a relatively short baseline.

2. TROUGH/OPTICS DESIGN

A horizontal half-filled fluid tiltmeter tank was selected because of its inherent temperature stability.[5] The tank is a simple, rectangular, 1-m long plexiglass tank. Tilt, in such a tank, is measured as the difference in liquid height between the ends of the tank. Changes in the liquid height can be measured by two separate optical interferometer systems, one at each end, that use a 256-element photodiode array detector. Comparing the two measurements results in a tilt signal. A mini-computer data acquisition system analyzes the data and periodically records and stores the changes in tilt.

Rather than use two interferometer systems, we decided to include both ends of the tank within the same interferometer system. This resulted in a simpler tiltmeter and also reduced the cost. It is important to note that, while this method works well for relatively short tanks such as ours, it may be impractical for very long baseline tiltmeters, because the optical beam would have to travel the length of the tiltmeter and could be affected by atmospheric and thermal fluctuations.

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5. Beavan, J., and Bilham, H. (1977) Thermally induced errors in fluid tube tiltmeters, J. Geophys. Res. 82 (No. 36).

The Mach-Zehnder interferometer optical system uses an unstabilized 5-mW He-Ne (Helium-Neon) laser as a light source. Using the dimensions ℓ and L in Figure 1 and assuming that the tiltmeter system (including the tank and optics) is tilted relative to the fluid surface by an angle Φ, the optical path difference (OPD) between the two paths of the interferometer is

$$OPD_{\Phi} = [L + (\ell - r - L\Phi) + n_{\omega}(r + L\Phi)] - [L + (\ell - r + L\Phi) + n_{\omega}(r - L\Phi)]$$

$$= n_{\omega} L\Phi - L\Phi = L\Phi(n_{\omega} - 1) \quad ,$$

where n_{ω} equals the index of refraction for the tank fluid, the index of refraction of air equals one ($n_a = 1$), and $L\tan\Phi \cong L\Phi$ for very small angles of Φ. The size of the tilt angle to be measured is generally very small. For example, the peak-to-peak tilt angle for the east-west component of the combined earth tides and ocean loading in the Boston, Mass. area is approximately 250 nrad.[6] In terms of the wavelength of the He-Ne laser light where $\lambda = 0.6328\ \mu m$,

$$OPD_{\Phi} = \frac{L\Phi}{\lambda}(n_{\omega} - 1) \text{ in wavelengths.}$$

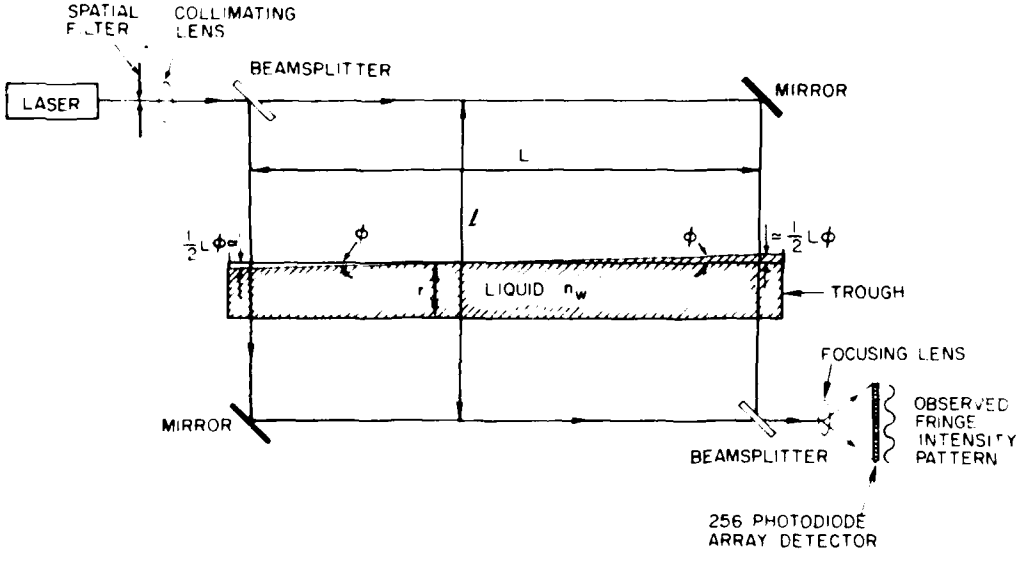

Figure 1. Optical Interferometer and Trough System

6. Cabaniss, G. H. (1978) The measurement of long period and secular deformation with deep borehole tiltmeter, Proc. 9th GEOP Conf., An International Symposium on the Application of Geodesy to Geodynamics, Dept. of Geodetic Science Report No. 280, The Ohio State University, Columbus, Ohio.

One interferometer output fringe shift corresponds to an OPD of one half a wavelength ($\lambda/2$). Therefore the optical detector actually observes a change of

$$\Delta_{\text{Fringes}_\Phi} = \Delta F = \frac{2L\Phi}{\lambda}(n_\omega - 1) \quad , \tag{1}$$

where ΔF is the fractional fringe shift observed by the optical detector. The total irradiance at the output of the interferometer is[7]

$$I = I_1 + I_2 + 2\, I_1 I_2 \cos\Theta \quad , \tag{2}$$

where I_1 and I_2 are the irradiance from the arms of the interferometer, and Θ is the phase difference between the two paths. The interferometer is adjusted so that straight line fringes of equal thickness (also called Fizeau fringes) are focused onto the optical detector (a 256-photodiode array with aperture size $\approx$ 4 mm) so that several cycles of the fringes are incident across the linear detector. Thus the detector "sees" several cycles of Eq. (2) directly. From Eq. (1),

$$\Phi_{\text{tilt}} = \frac{\lambda(\Delta F)}{2L(n_\omega - 1)} \quad ; \tag{3}$$

and, using $\lambda = 0.6328\ \mu$m (He-Ne), L = 1 m, $n_\omega = 1.33$ (water),

$$\Phi = (0.959)\,\Delta F \ \ \mu\text{rad} \quad . \tag{4}$$

Thus, the observed interferometer fringe shift is proportional to the angular tilt that caused the fringe shift. The highest resolution attainable, therefore, depends on the smallest fractional fringe shift that can be observed, and this is only limited by the amplitude size of the optical and electrical noise. For example, if one complete fringe cycle fills the 256-photodiode array and a fringe shift over two photodiodes is distinguishable, then the resolution of the tiltmeter would be

$$\Phi \sim \Delta F\ \mu\text{rad} = (0.959)(2/256)\ \mu\text{rad} = 0.00750\ \mu\text{rad} = 7.50\ \text{nrad} \quad .$$

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7. Hecht, E., and Zajac, A. (1974) Optics, Addison-Wesley Publishing Co., Reading, Mass., p. 278.

3. DATA ACQUISITION SYSTEM

The data acquisition system of the long baseline tiltmeter (LBT) consists of the optical detector and associated electronics necessary for transferring the interferometer fringe intensity pattern from the detector to: a Digital Equipment Corporation (DEC) LSI-11 computer, a real-time clock (part of the LSI-11 computer), a digital thermometer that records the temperature around the tiltmeter, and a floppy disk system for mass storage of tilt data (Figure 2). The optical detector and associated electronics are separated into five subsystems: (a) the optical detector, which is a 256-photodiode array housed on a motherboard that converts the interferometer fringe intensity pattern into an analog video signal, (b) an analog-to-digital converter that digitizes the analog video signal, (c) a data buffer for temporary storage of the digital data, (d) a line current driver interface that drives the digital signal through a ribbon cable to the LSI-11 computer, and (e) the timing circuitry necessary to synchronize the flow of data from the sensor, through the subsystems, to the computer. All of the five subsystems, except for the detector/motherboard, are housed in a 5.25-in. card cage mounted in a standard 19-in. equipment rack. The detector/motherboard is connected to the card cage by an extension card through a 25-in. cable strand (Figure 3). This allows some freedom in placing the detector close to the interferometer.

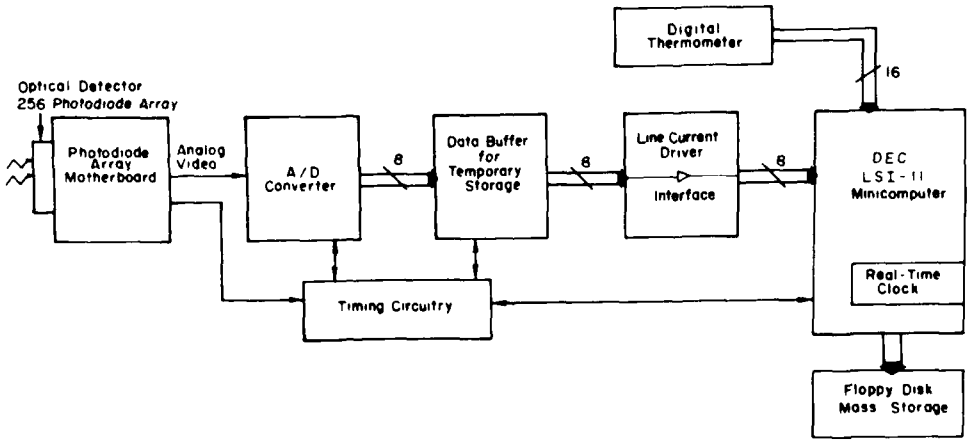

Figure 2. Data Acquisition System Block Diagram

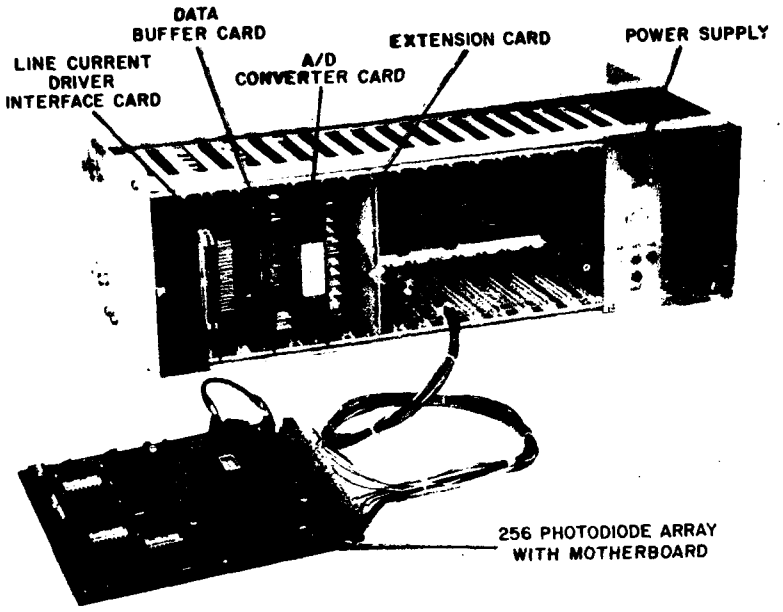

Figure 3. Photograph of Card Cage for Optical Detector and Electronics

3.1 Optical Detector

The optical detector, a CCPD (Charge Coupled Photodiode) 256-pixel array manufactured by EG&G Reticon, is a linear array of p-n junction photodiodes that are spaced on 16-μm centers with a total aperture of 4.096 mm.[8] The array is mounted on a 22-pin dual-in-line ceramic package under a ground and polished window (Figure 4). The 22-pin package is soldered onto the RC702A satellite board that is directly connected to and rides piggy-back on the RC700A motherboard (Figure 5). The CCPD 256 array and the RC702A/RC700A boards (all manufactured by EG&G Reticon) make up the CCPD interface system that provides timing, video processing, and blanking requirements for the CCPD array. Figure 6 is a simplified block diagram of the CCPD array and RC702A/RC700A boards.[9]

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8. Charge Coupled Photodiode Arrays CCPD-256 or CCPD-1024 (1979) Data Sheet No. 08088, EG&G Reticon, Sunnyvale, Calif.

9. RC702A/RC700A CCPD Interface System Operating Instructions (1979), Document No. 045-0042, Reticon Corporation, Sunnyvale, Calif.

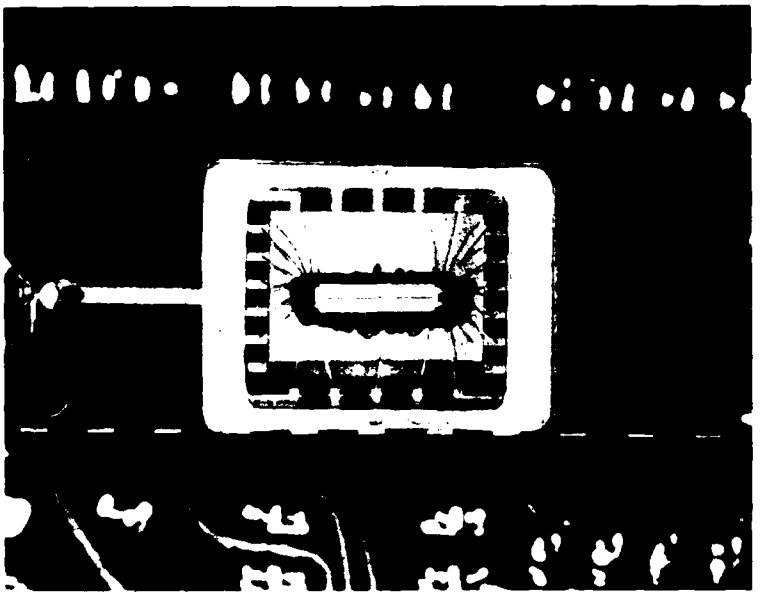

Figure 4. Photograph of CCPD 256-Photodiode Array

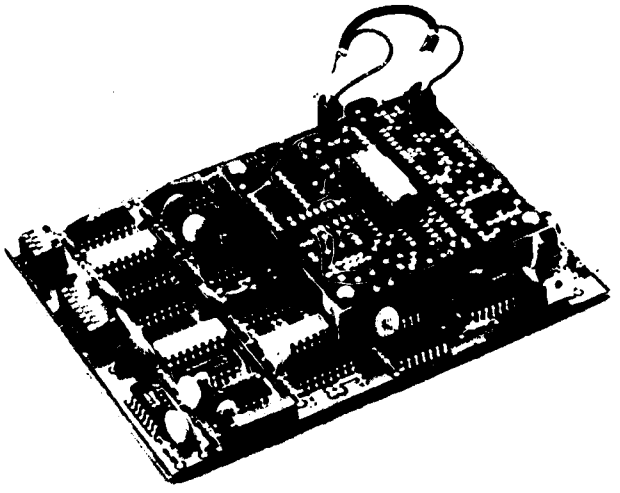

Figure 5. Photograph of RC702A Satellite Board With CCPD 256-Photodiode Array Attached to the RC700A Motherboard

As shown in Figure 6, one complete scan of the CCPD 256-photodiode array consists of:[8, 9] incident light on each p-n junction photodiode that generates photocurrent, which is integrated by and stored in the capacitance of each photodiode; the voltage stored is proportional to the integrated intensity. If the accumulated voltage exceeds a certain saturation level, the excess charge is shunted off each photodiode by anti-blooming gates, thus avoiding blooming effects.* At the end of the integration period, the 256 charges are transferred to two CCD analog shift registers; even photodiodes are transferred to one register, and odd photodiodes are transferred to the other. Immediately after this transfer, a new integration period begins. The two CCD shift registers are then alternately clocked by the four-phase clock to generate a 256-pixel analog video data stream. Each consecutive pixel corresponds to each consecutive photodiode. The relative amplitude of the odd and even parts is adjusted by the odd-even balance potentiometer. After initial amplification, each pixel is held by the sample-and-hold circuit for a specific time duration. At the end of the 256-pixel data stream, the dc restoration switch is closed, reestablishing a ground reference to the video signal. The

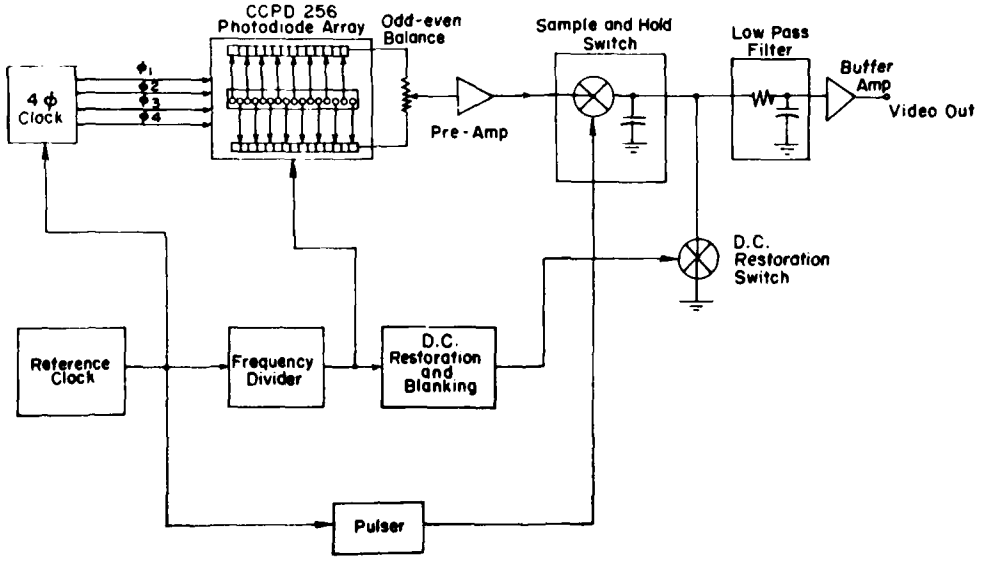

Figure 6. Simplified Block Diagram of CCPD 256-Photodiode Array, RC702A Satellite Board, and RC700A Motherboard

*Blooming refers to leakage from one or several saturated photodiodes to neighboring photodiodes such that the saturated level spreads beyond the group of locally affected cells. Blooming effects are common in multi-celled imaging devices.

signal passes through a low-pass filter that reduces high-frequency switching spikes from the sample-and-hold switch and the dc restoration switch. The final buffer amplifies the video signal to approximately 2.4 V peak-to-peak when the array is saturated.

The frequency of the reference (master) clock on the RC700A motherboard has been changed from the factory-set value of 1.5 MHz to approximately 120 kHz to accomodate the analog-to-digital converter speed. This modification consists of changing oscillator capacitor C1 to 300 pF and C20 to 0.1 μF on the RC700A motherboard.[10] (The schematic of the RC702A/RC700A boards are not contained in this report, however they may be found in Refs. 8 and 9.) The time for one complete scan is approximately 4.4 msec or 227 complete scans per second when the new clock frequency is approximately 120 kHz and the integration period is set to the minimum amount as described in Ref. 9. Within each scan, the time for each video pixel is 16 μsec.

3.2 Analog/Digital Converter Board

The analog-to-digital (A/D) converter board houses the analog-to-digital converter circuit and all of the timing circuitry necessary for synchronizing the A/D conversion with the video data coming from the CCPD motherboard. The block diagram of the A/D converter board, Figure 7, shows the overall view of how the components are interconnected. The actual circuit schematic is in Figure 8. Figure 9 is the timing diagram of the important digital signals used in the A/D conversion.

The analog-to-digital converter (U2), manufactured by Micro Network Corporation, is a MN5123 8-bit converter. The input voltage range is 0 to 10 V. If converted to an 8-bit digital byte, it corresponds to 00000000 to 11111111 binary or 00 to FF hexidecimal. It can complete a conversion in 6 μsec with $\pm$ least significant bit (LSB) linearity. There are no gain or offset adjustments necessary when the operating temperature range is 0 to 70°C.

As mentioned before, the video signal from the CCPD motherboard has a maximum value of approximately 2.4 V when fully saturated. In order to match the input voltage range of the A/D converter of 0 to 10 V, the video signal is multiplied by a factor of four by a noninverting amplifier using an RCA CA3130AE operational amplifier (U1). A second CA3130AE is used as a unity-gain buffer between the amplified video signal and a BNC connector labelled "monitor" on the A/D converter board. This allows the operator to monitor the video signal directly with the use of an oscilloscope for alignment purposes.

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10. Von Glahn, P. G., Capt. (1981) private communication.

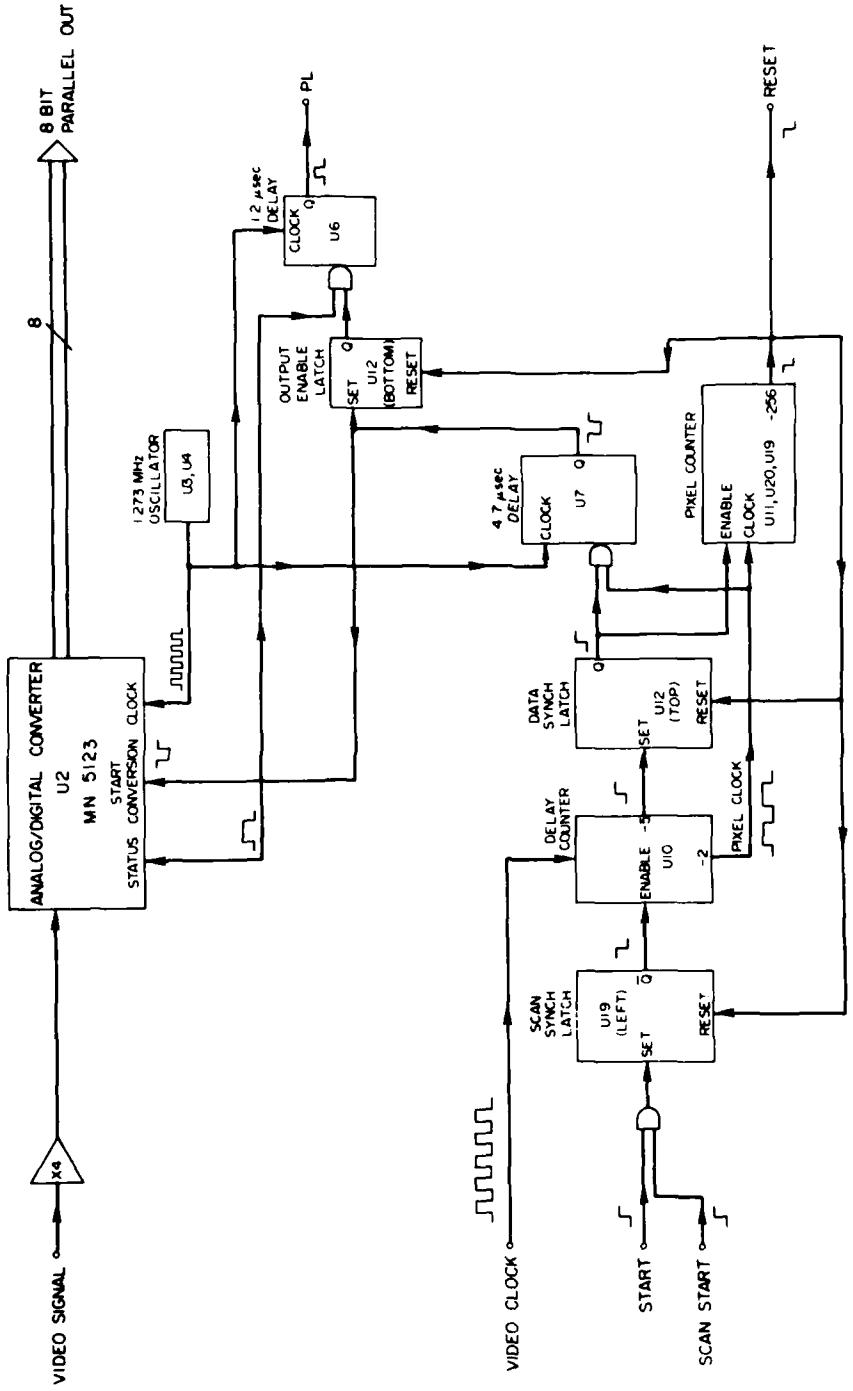

Figure 7. Block Diagram of A/D Converter Board

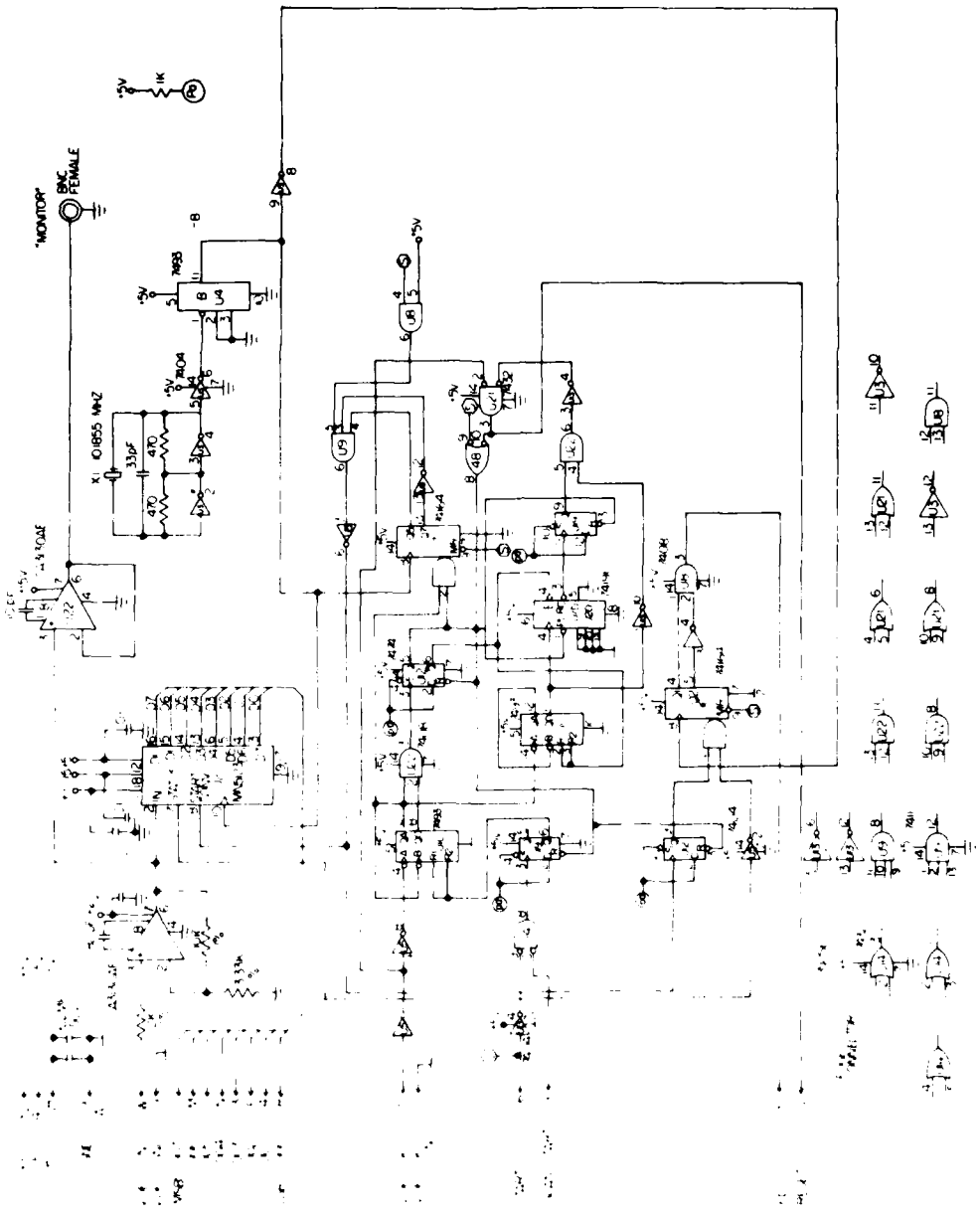

Figure 8. Schematic of A/D Converter Board

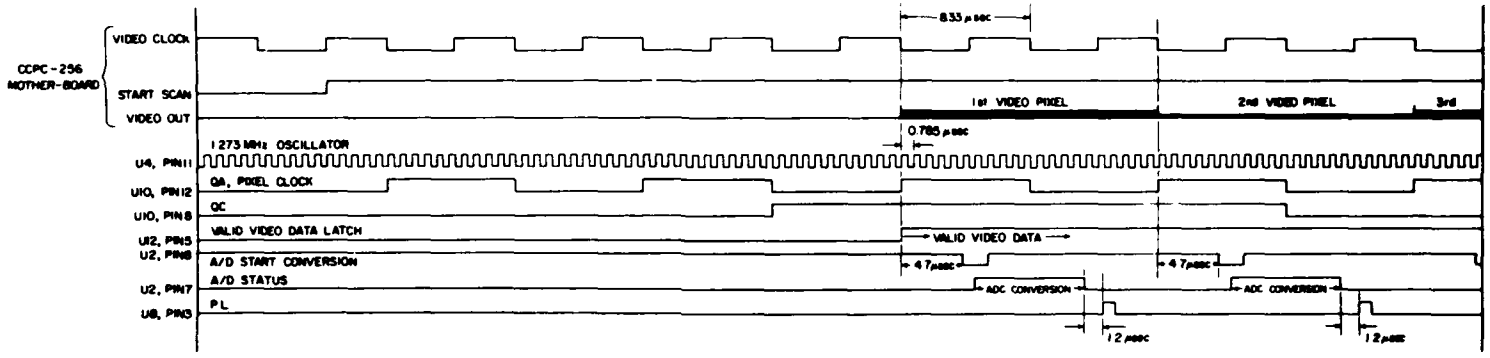

Figure 9. Timing Diagram of Analog-to-Digital Conversion

Referring again to Figures 7 and 8, the video signal, video clock, and the SCAN START lines all come from the CCPD motherboard. The video clock frequency is twice that of the pixel frequency of the video signal, and is used by the timing logic to synchronize the A/D conversion with valid video data. The SCAN START digital line changes from a low state to a high state (0 to 1) five video clock pulses before the first video pixel is valid (see Figure 9). The SCAN START line stays at a high state (1) during one entire 256-video pixel scan, then changes back to a low state (0) and stays low during the integration period of the photodiode array. The SCAN START line then goes high again, signaling the next photodiode array video scan. As mentioned earlier, there are approximately 227 video scans per second, therefore the SCAN START line also pulses 227 times a second.

Although not every video scan is digitized, the START digital line selects those that are by gating the SCAN START line. The START line comes from the FIFO data buffer board (Figure 10). It is normally at a low state, but can be set high under computer control. The INITIATE digital line shown in Figure 10 is normally low, but is set high under direct computer control. This low-to-high INITIATE transition sets latch U16, thereby setting the start line high. It then goes to the A/D converter board to gate the next SCAN START pulse, setting the scan synch latch (shown in Figures 7 and 8) and enabling the electronics to digitize the following video scan. The setting of the scan synch latch (U19, left) enables the delay counter (U10) to start dividing the video clock frequency. The QA output of the delay counter, called the pixel clock, is the video clock frequency divided by two. The QC output of the delay counter, when added together by gate U22 with QA, gives a pulse that is the video clock divided by five. This then sets the data synch latch (U12, top). The rising edge of the Q output of the data synch latch, as seen from the timing diagram, marks the time when video data is valid on the video signal line. The pixel clock frequency, which is the same as the video pixel data, is gated by the data synch latch output to U7 [a shift register set up to strobe the A/D converter (U2) after a 4.7-μsec delay]. The delay allows for analog data settling on the video signal line.

The negative-going pulse from U7 strobes the A/D converter to start the analog-to-digital conversion in addition to setting the output enable latch (U12). During the conversion time, the STATUS line from the A/D converter is high. At the end of the conversion, the STATUS line goes low, triggering U6 (also a shift register) to generate a strobe pulse after a 1.6-μsec delay. This pulse on the PL (parallel load) line is used on the FIFO data buffer board to strobe the 8-bit parallel digital byte into the data buffer memory.

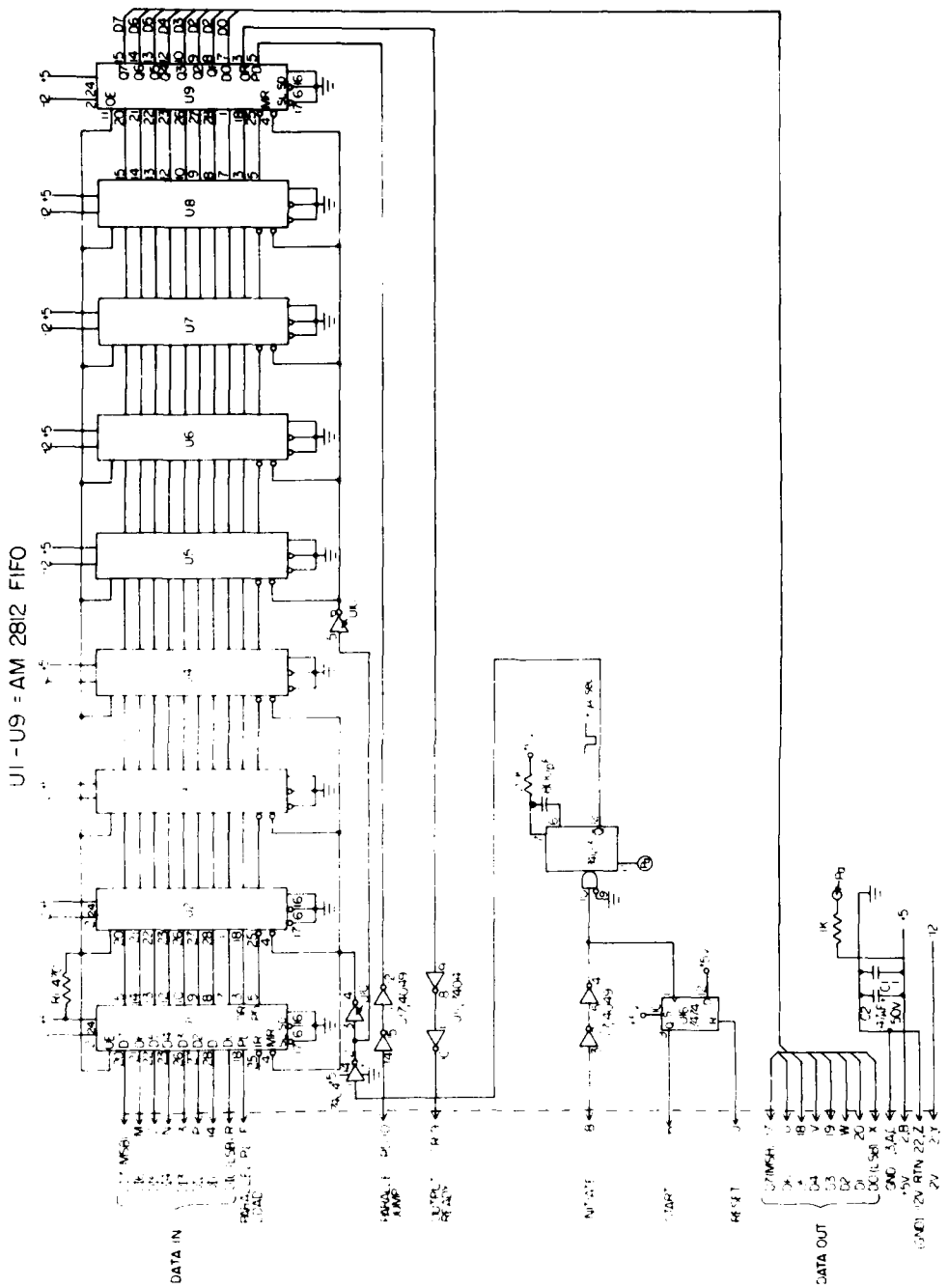

Figure 10. Schematic of FIFO Data Buffer Board

During the 256-pixel video scan, the pixel clock continues to trigger U7, which strobes the A/D converter to digitize each analog pixel. The pixel counter (U11, U20, and U19) counts the pixel clock pulses, and, after 256 counts, generates a scan reset level transition that resets all of the latches and forces the A/D conversion process to stop. The scan reset also resets the latch on the FIFO data buffer board (U16) so that the START line goes low and is ready to be set high again upon command from the computer.

The A/D converter (U2) and the two shift registers (U6 and U7) all receive their clock timing signals from the clock oscillator made up of U3, U4, and a crystal. The oscillator itself generates a 10.1855-MHz frequency that U4 divides by 8 to give a clock frequency of 1.273 MHz. This 1.273-MHz signal drives the A/D converter's clock, which, by specifications, must be below the maximum value of 1.33 MHz. The 1.273-MHz signal also drives the two shift registers, U6 and U7, and is responsible for the 4.7- and 1.2-μsec delays introduced by them respectively.

3.3 FIFO Data Buffer Board

The FIFO (first-in first-out) data buffer board houses the digital memory circuits that temporarily store a complete video scan consisting of 256 8-bit bytes. After temporary storage, the 256 bytes are sent to the LSI-11 computer through the line current driver interface board. Temporary storage of the video data bytes is required, because the computer cannot respond fast enough to receive consecutive bytes spaced by only 16 μsec.

The memory circuits consist of nine Am2812 32×8-bit FIFO memory integrated circuits manufactured by Advanced Micro Devices (see Figure 10). The Am2812 memory circuit has completely independent read and write controls with input and output rates up to 1 MHz. A strobe pulse on the PL line (generated on the A/D converter board) writes an 8-bit data byte into the memory. The data byte automatically ripples through the memory registers until it reaches the output or another data byte previously stored. When a data byte is available on the output of the FIFO, the OR (output ready) line goes high, indicating valid data. The data byte is read from the FIFO by applying a pulse on the PD (parallel dump) line. When this occurs, the rest of the stored bytes ripple down to the end of the FIFO. The timing signals are designed so that two or more FIFOs can be connected together to multiply the memory capacity. However, because of a peculiarity in the design, FIFOs storing 32×n bytes only store 31×n + 1 bytes.[11]

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11. Am2812/Am2812A, Am2813/Am2813A, 32×8-Bit and 32×8-Bit First-In First-Out Memories (1974), Data Sheet, Advanced Micro Devices Inc., Sunnyvale, Calif.

Therefore, nine FIFOs will give a total storage of 280 bytes, where the lowest multiple is equal to or greater than 256.

When the INITIATE line goes high (under computer control by setting the CSRO line high on the DRV-11 parallel interface on the LSI-11 computer, see Figure 11) to initiate a video scan sequence, the rising edge triggers a monostable multivibrator (one-shot, U11). This generates a negative-going 6-μsec pulse and clears the memory registers of the nine FIFOs by pulling the MR (master reset) line low. The arriving video data bytes then ripple down the empty

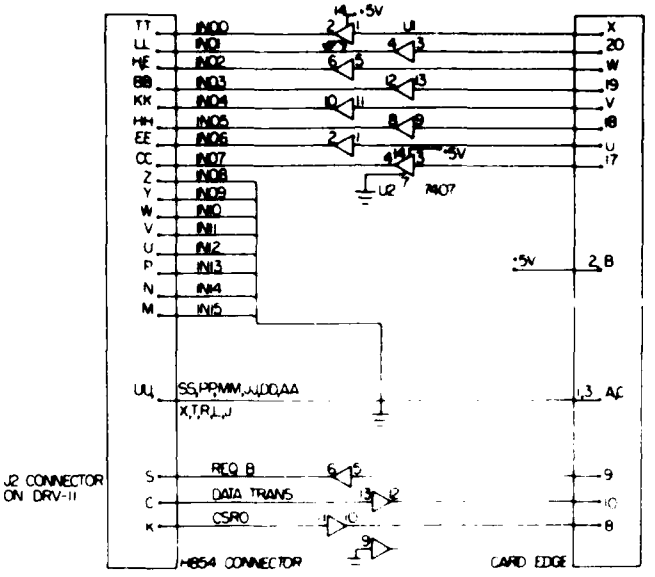

Figure 11. Schematic of Line Current Driver Interface Board

FIFOs to the output of the last FIFO, U9, and the 256 bytes stack up in the memory row and the first FIFO, U1. The arrival of the first video byte at the output of FIFO U9 sets the OR line high, which in turn sets the *REQ B* line (see Figure 11) of the DRV-11 parallel interface high and tells the LSI-11 computer that video data is available to be read. The computer then reads a data word (bits 0-7 are the video byte, bits 8-15 are set to 0) and sends a transfer pulse, acknowledging that the reading is complete, out of the DRV-11 on the DATA TRANS line.[12] This

12. Microcomputer Interfaces Handbook (1980), Digital Equipment Co., Maynard, Mass.

pulse travels to the PD line of the last FIFO, U9, and ripples the rest of the video data bytes down to the end of FIFOs, thereby setting the next video data byte available to be read by the computer. Since the read time of the LSI-11 computer is much slower than the write time of the video data into the FIFOs, only a few data bytes will have been read by the time the 256th byte is written into the FIFOs.

3.4 Line Current Driver Interface Board

The line current driver interface board (Figure 11) is the interface between the FIFO data buffer board and the DRV-11 parallel interface board on the LSI-11 computer. The purpose of the interface is to boost the current level of the video and control digital signals through the ribbon cable between the card cage and the LSI-11 computer.

3.5 Electronics Power Supply and Backplane

The power supply (Figure 12) supplies all the dc power requirements for the LBT electronics in the card cage including the CCPD motherboard. The power supply consists of three separate supplies: A PSI Power Products Co. HE-237 10 Amp unit provides 5 V dc for all the logic circuits; plus and minus 15 V dc for the A/D converter, video amplifiers and the CCPD motherboard comes from a Semiconductor Specialists Co. P2.15.200 200 mA ±15 V unit; and minus 12 V dc, needed by the FIFO memories, is supplied by a simple 12-V regulated full-wave rectified power supply. The wiring diagram of the backplane in Figure 13 shows how the various boards in the card cage are interconnected.

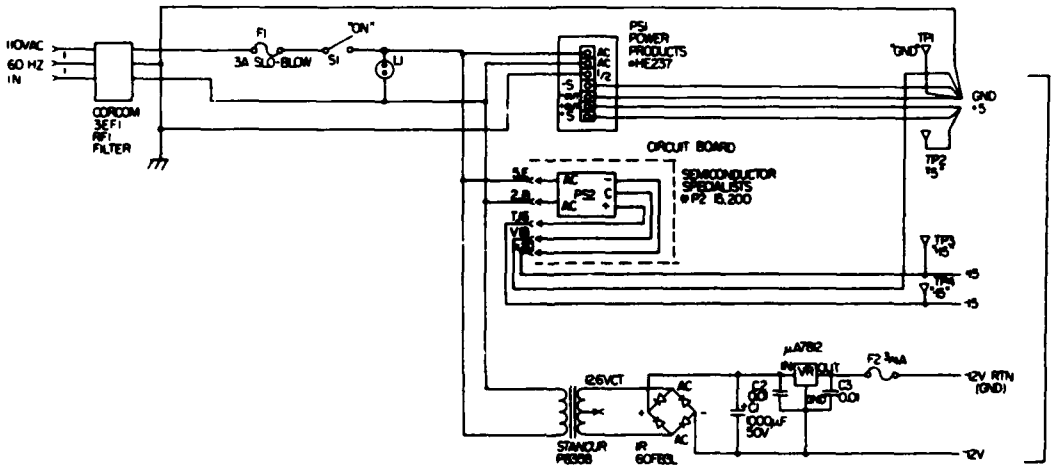

Figure 12. Schematic of Electronics Power Supply

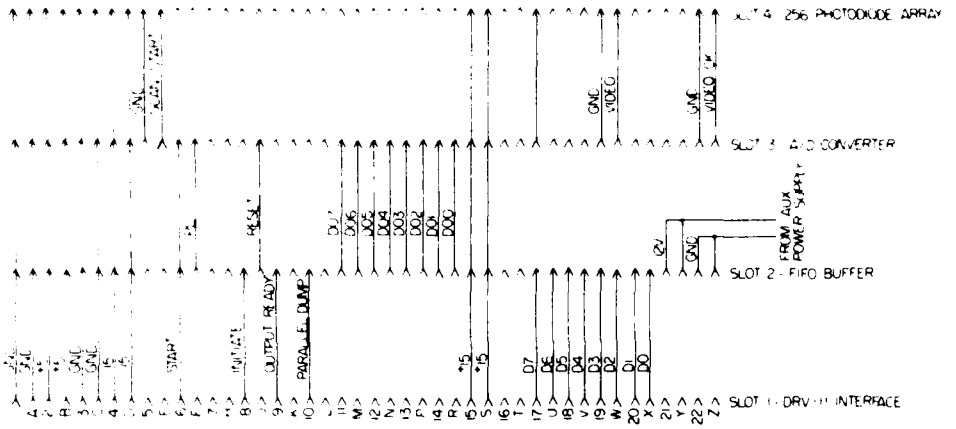

Figure 13. Schematic of Card Cage Backplane

3.6 Digital Thermometer and Interface

The digital thermometer, Model 5510 manufactured by Digitec Instrumentation, is used to monitor the changes in temperature around the tiltmeter (see Figure 14). It can display temperature in either Centigrade or Farenheit, and has an accuracy of 0.42°C (on the -30.00° to +50.00°C range) or 0.72°F (on the -22.00° to +122.00°F range). The repeatability of the thermometer is 0.01. This is significant because, for this application, the change in temperature is most important and not the absolute temperature. The thermister probe is attached to the thermometer through a 6-ft cable.[13]

The thermometer has a built-in digital interface for a connection to a computer. Figure 15 shows the wiring between the thermometer connector J3 and a DRV-11 parallel interface to the LSI-11 computer. The thermometer output is a four-digit BCD (binary coded decimal) output in which the temperature, as shown in Figure 15, is encoded. To read the temperature, the computer (through the DRV-11 interface) pulls the CSRO line low, triggering the thermometer to take a temperature reading. The thermometer responds by setting the BUSY line high

13. Models 5510 & 5530 Thermometers, Equipment Manual, Digitec Instrumentation, United Systems Corp., Dayton, Ohio.

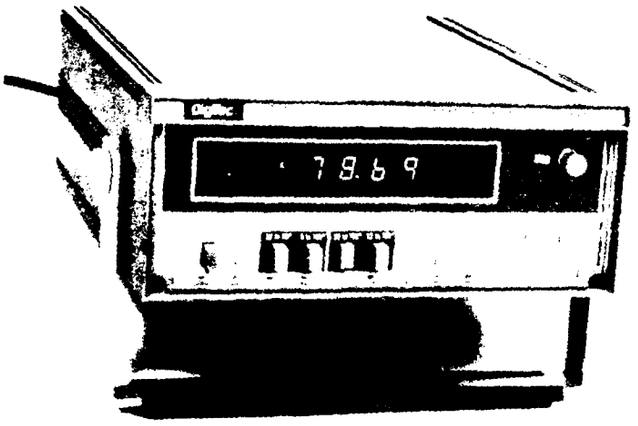

Figure 14. Photograph of Digitec Model 5510 Digital Thermometer

during the reading. At the end of the reading, which takes from 1 to 2 msec, the BUSY line drops back low, thus informing the computer that valid data is available. The computer subsequently reads the BCD encoded digital temperature word.

3.7 LSI-11 Computer

As previously mentioned, the LSI-11 computer system is made up of the following: the LSI-11 computer (consisting of the backplane and various modules), a floppy disk for mass storage, and a graphics terminal. Table 1 lists the modules that are necessary for operation of the tiltmeter. Table 2 shows the input/output

Table 1. LSI-11 Computer Modules

Module	Function
LSI-11	System computer
32K RAM	Computer memory with console terminal serial port
RXV-21	Double density floppy disk controller
DRV-11	Tiltmeter electronics parallel interface
DRV-11	Thermometer parallel interface
Q-Timer	Real-time clock

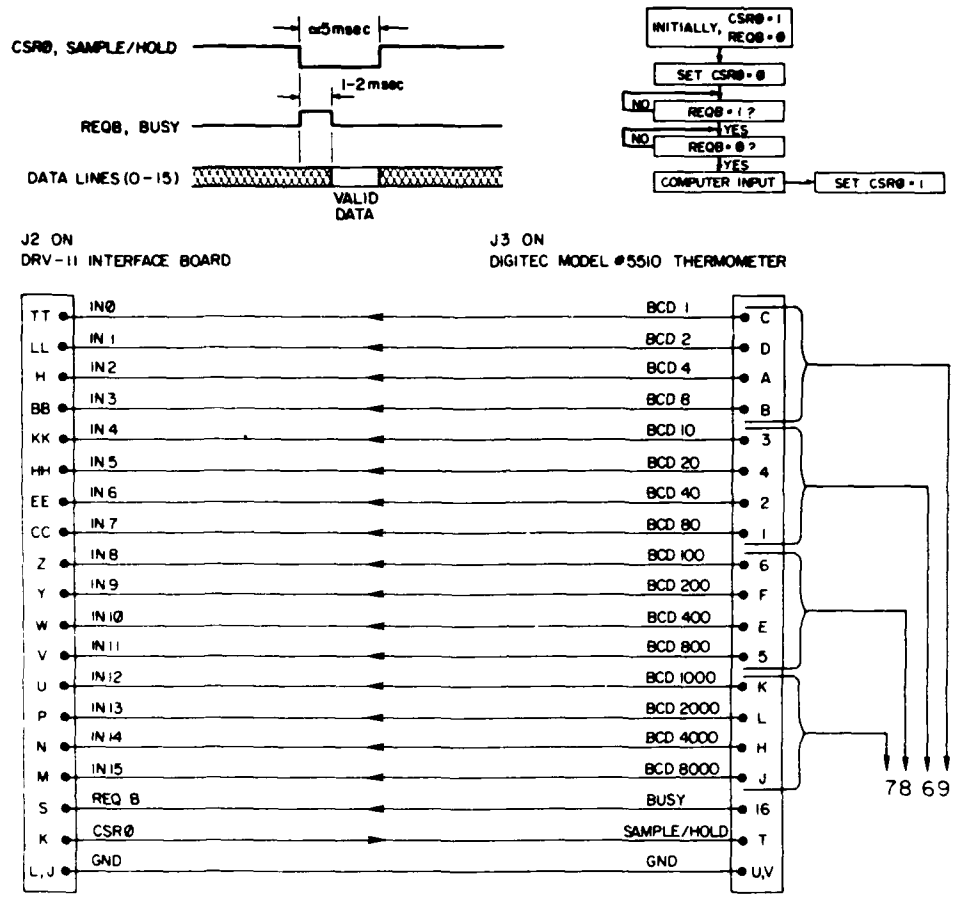

Figure 15. Schematic of Digital Thermometer — DRV-11 Interface

(I/O) module register addresses used in the LSI-11 computer memory. The Q-timer module is a bettery back-up real-time clock that can be set under operator control and is read under program control through access to the Q-timer clock registers in Table 2. The terminal used is a GX-100 graphics terminal (768 × 585 resolution) manufactured by Modgraph Inc. It features graphics compatible with the Tektronix 4010 and text editing compatible with the DEC VT-100.

Table 2. Input/Output Module Register Addresses

Address	Function	Bits Used
167760	Tiltmeter electronics CSR*, [12]	0-15
167764	Tiltmeter electronics input buffer	0-15
167770	Temperature CSR	0-15
167774	Temperature input buffer	0-15
177304	Q-Timer clock seconds (units)[14]	0, 1, 2, 3
177306	Q-Timer clock seconds (tens)	0, 1, 2
177310	Q-Timer clock minutes (units)	0, 1, 2, 3
177312	Q-Timer clock minutes (tens)	0, 1, 2
177314	Q-Timer clock hours (units)	0, 1, 2, 3
177316	Q-Timer clock hours (tens)	0, 1
177320	Q-Timer clock days (units)	0, 1, 2, 3
177322	Q-Timer clock days (tens)	0, 1
177324	Q-Timer clock day of week	0, 1, 2
177326	Q-Timer clock month (units)	0, 1, 2, 3
177330	Q-Timer clock month (tens)	0
177560	Console receiver CSR	7-15
177562	Console receiver buffer	0-15
177564	Console transmitter CSR	0-15
177566	Console transmitter buffer	0-15

*Control Status Register (CSR)

3.8 Tiltmeter Software and Operation

The LSI-11 computer uses the Digital Equipment Corporation (DEC) RT-11SJ Version 4.0 operating system. All of the software, except for the primitive graphics routines that are written in RT-11 MACRO assembly language, are written in FORTRAN IV. The driving program for the tiltmeter reads the tiltmeter data, analyzes it, and writes it into a data file on a floppy disk. This program consists of a main menu for operator selection of various functions and 14 subroutines for performing the various tasks. Figure 16 is the flow diagram for collecting tiltmeter data. The operator can display the current time and date, and the filtered or unfiltered 256-photodiode scan vs intensity plot on the computer terminal (see Figure 17), and can engage the tiltmeter data collection at any sample rate from two to ten minutes (sample rates as low as ten seconds can be programmed into the computer). Figure 18 shows a fringe shift between two fringe patterns. The fractional fringe shift [ΔF in Eq. (4)], as measured in Figure 18 between the trough positions, is equal to X/D. Figure 19 shows raw tilt data taken over a two-day period. This figure is a plot of two adjacent trough positions as they move over time. It does not represent tilt; however, it is related to tilt through the fractional fringe shift previously mentioned. Two corrections are

14. Q-Timer User's Manual (1983), Document No. 131-0100-01, Codar Technology Inc., Longmont, Colo.

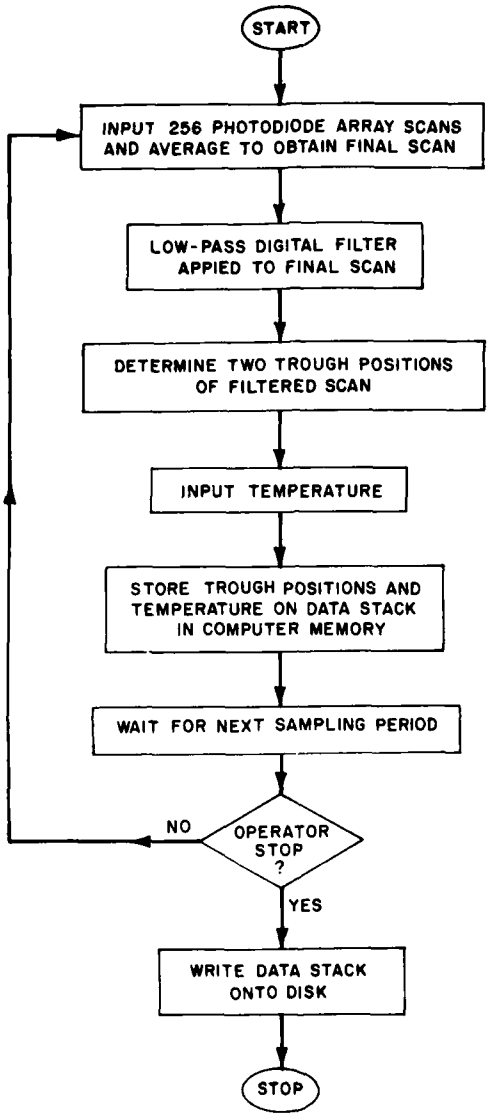

Figure 16. Software Flow Diagram of Tiltmeter Data Acquisition

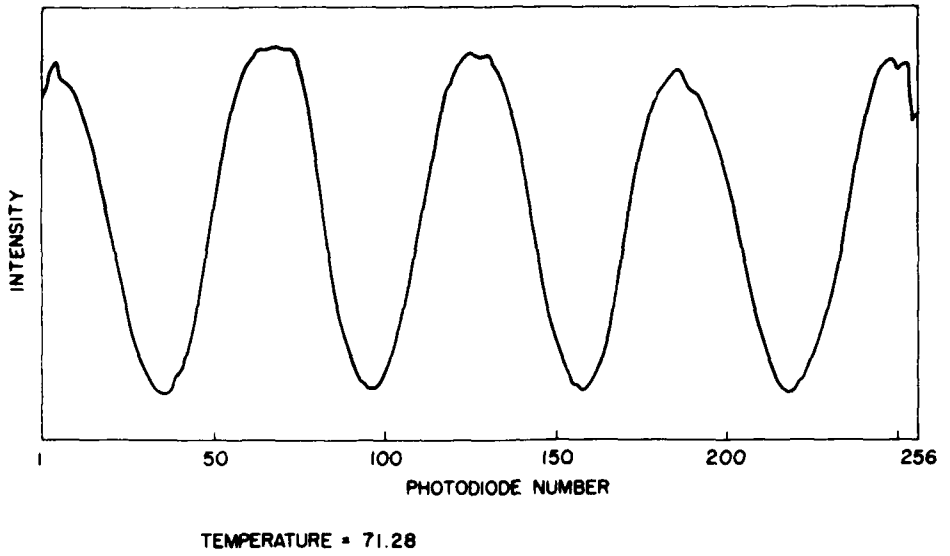

Figure 17. Computer Display of Filtered Photodiode Array Fringe Pattern

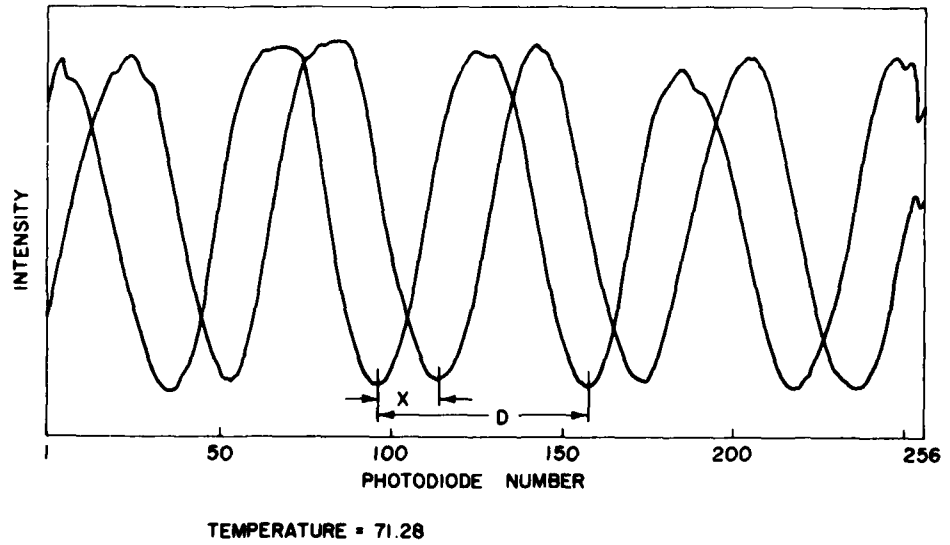

Figure 18. Computer Display of Two Fringe Patterns Superimposed Showing a Fringe Shift Between Them

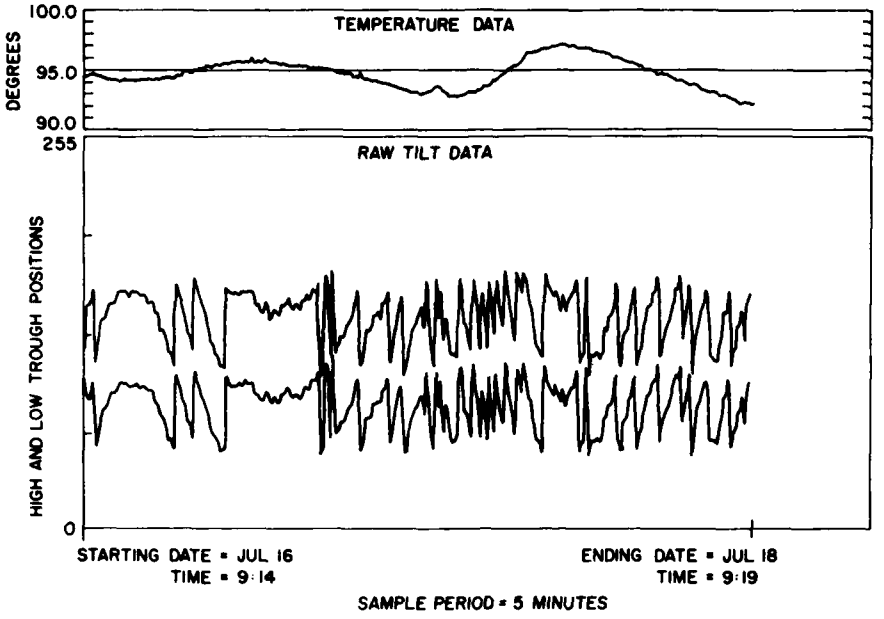

Figure 19. High and Low Trough Positions Over a Two-Day Period (Raw Tilt Data)

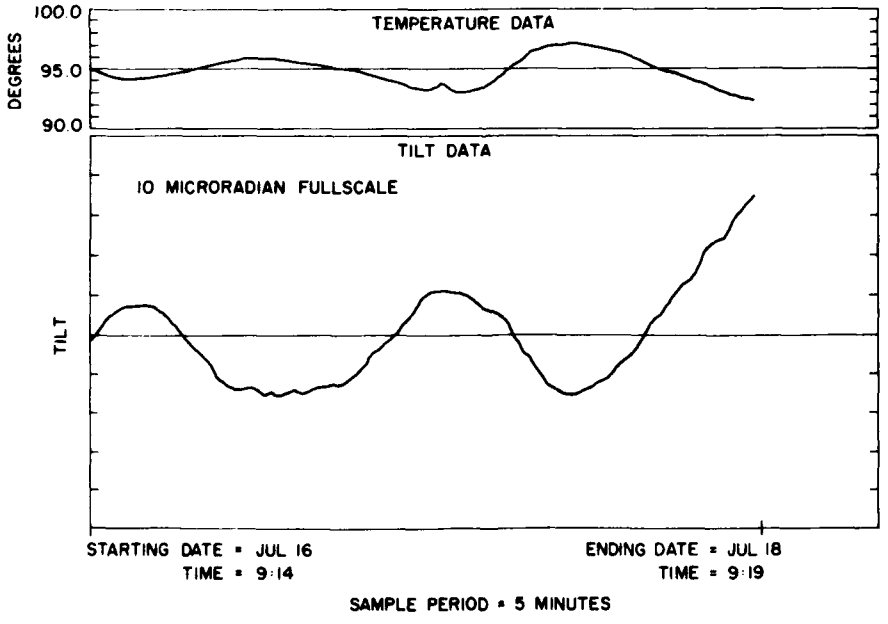

Figure 20. Calculated Tilt Signal Over Same Two-Day Period

necessary to calculate the actual tilt. First, noise spikes, which occur when the computer algorithm jumps from one fringe trough to an adjacent one, must be eliminated. Secondly, the effects of fringe pattern shifts (where the computer algorithm must jump to an adjacent fringe in order to track the signal) must also be eliminated. Figure 20 is a scaled diagram showing the calculated tilt signal over a two-day period after the effects were removed. The variation of the temperature around the tiltmeter is also shown. Visual observation of the tile and temperature curves show a strong correlation between the two. Judging from the amplitude size of the tile signal (over two μrad peak-to-peak), the signal must be significantly related to temperature since the amplitude of the earth tides is less than one-half a μrad.

4. CONCLUSIONS

Due to unforeseen equipment malfunctions, the current prototype tiltmeter has only been in operation for a short time. However, the photodiode array detector and the electronics design have performed satisfactorily and dependably. In order to build a multidetector computer system, other photodiode arrays could be connected to the analog-to-digital converter through analog switches. This optical detector system could then be used for other projects requiring the use of a linear-array detector.

The mechanical tiltmeter (trough and optics) requires more work to eliminate the temperature dependence. This could be accomplished either by controlling the temperature variations around the tiltmeter to less than a fraction of one degree or by compensating for the temperature fluctuations (preferably both). One promising method would be to build another interferometer into the existing one: this would only measure movement of the optics due to temperature, material stress, or creep, and would be insensitive to the tilt signal. An example of such an interferometer is the Sagnac interferometer, which is very similar to the Mach-Zehnder interferometer. The only difference is the position of one mirror; however, with specialized optics design, a cube-beam-splitter could be made to satisfy both types of interferometers. The Sagnac interferometer, due to the double-ring property of the optical paths, would be insensitive to a tank of liquid placed between its two paths, and would only sense rotations of the optics.

The length of the tiltmeter tank, of course, is very important, since this amplifies the tilt signal to be measured. A tiltmeter of this design must always be kept indoors in order to protect the laser and liquid tank. This, however, limits the size of the tiltmeter length, unless a long vault is used.

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